Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (previously presented): A compensating apparatus for compensating for intermodulation products, the apparatus comprising:

a phase splitting unit, which splits an input RF signal into an in-phase component and a quadrature component;

first multiplying units, which square the value of the in-phase component and the quadrature component respectively;

a first summer which sums the squared values to generate an X^2 signal;

combining units, which respectively combine the X^2 signal, the in-phase component, the quadrature component, and an external signal with respective predistorting coefficients; and

an adder, which generates a predistored RF signal from the output of the combining units.

Claim 2 (currently amended): A compensating apparatus according to claim 1, wherein the combining units comprise first to sixth combining units,

the first ~~combination~~ combining unit combining the X^2 signal with a first predistorting coefficient;

the second combining unit combining the X^2 signal with a second predistorting coefficient;

the third combining unit combining the external signal with a third predistorting coefficient;

the fourth combining unit combining the external signal with a fourth predistorting coefficient;

the fifth combining unit combining the in-phase component with a fifth predistorting coefficient;

the sixth combining unit combining the in-phase component with a sixth predistorting coefficient.

Claim 3 (previously presented): A compensating apparatus according to claim 2, further comprising a second summer summing the outputs of first and third combining units; and a

third summer summing the outputs of second and fourth combining units.

Claim 4 (previously presented): A compensating apparatus according to claim 3, further comprising a second multiplying unit which multiplies the output of the second summer with the in-phase component; and a third multiplying unit which multiplies the output of the third summer with the quadrature component, and wherein the adder sums the outputs of the first combining unit, the sixth combining unit, the second multiplying unit and the third multiplying unit to produce a predistorted RF signal.

Claim 5 (previously presented): A compensating apparatus as claimed in claim 1, wherein the apparatus is an application specific integrated circuit.

Claim 6 (previously presented): A compensating apparatus as claimed in claim 1, wherein an output carrying the X^2 signal is coupled to a delay unit and the output of the delay unit is fed back into the apparatus as the external signal, whereby the external signal is a delayed signal derived from the X^2 signal.

Claim 7 (previously presented): A compensating apparatus as

claimed in claim 1, the apparatus comprising a further multiplier, which squares the X^2 signal again to give a X^4 signal, wherein the external signal is the X^4 signal.

Claim 8 (withdrawn): A hybrid compensating apparatus for substantially simultaneously compensating for both carrier frequency and envelope frequency dependent effects due to IM3 products, the hybrid apparatus comprising:

a first compensating apparatus, comprising an ASIC, arranged to compensate for envelope frequency effects;

a second compensating apparatus, arranged to compensate for carrier frequency effects;

a carrier delay unit, which imposes a predetermined delay upon the RF input signal supplied to the second compensating apparatus; and

a further adder which sums the outputs of the first and second compensating apparatuses.

Claim 9 (previously presented): A feed forward amplifier arrangement comprising:

a compensating apparatus as claimed in, claim 1;

an amplifier having non-linear transfer characteristics that distort signals amplified thereby, the amplifier being coupled to the output of the compensating apparatus;

a controller which generates coefficients for feeding into the compensating apparatus; and

a sampling means which samples an output signal from the amplifier and which feeds the sample back to the controller.

Claim 10 (previously presented): A method of compensating for intermodulation products, the method comprising:

splitting an input RF signal into an in-phase component and a quadrature component;

squaring the in-phase component and quadrature component respectively and summing their squares to generate an X^2signal;

combining the X^2 signal, the in-phase and quadrature components, and an external signal with respective predistorting coefficients; and

generating a predistorted RF signal.

Claim 11 (previously presented): A method according to claim 10, wherein the combining step comprises first to sixth combining operations,

the first combining operation combining the X^2 signal with a first predistorting coefficient;

the second combining operation combining the X^2 signal with a second predistorting coefficient;

the third combining operation combining the external signal with a third predistorting coefficient;

the fourth combining operation combining the external signal with a fourth predistorting coefficient;

the fifth combining operation combining the in-phase component with a fifth predistorting coefficient;

the sixth combining operation combining the in-phase component with a sixth predistorting coefficient.

Claim 12 (previously presented): A method according to claim

11, further comprising a second summing operation of summing the results of first and third combining operations; and a third summing operation of summing the results of second and fourth combining operations.

Claim 13 (previously presented): A compensating apparatus according to claim 12, further comprising a second multiplying operation which multiplies the output of the second summing operation with the in-phase component; and a third multiplying operation which multiplies the output of the third summing operation with the quadrature component, and wherein the step of generating a predistorted RF signal comprises summing the results of the first combining operation, the sixth combining operation, the second multiplying operation and the third multiplying operation.

Claim 14 (previously presented): A method as claimed in claim 10, wherein the external signal is a delayed signal derived from the X^2 signal.

Claim 15 (previously presented): A method as claimed in claim 10, wherein the method further comprises squaring the X^2signal to generate a X^4 signal and wherein the external signal is the X^4 signal.

Claim 16 (canceled)

Claim 17 (new): The compensating apparatus of claim 1, wherein the respective predistorting coefficients are provided to the combining unit from a microcontroller performing a search algorithm.

Claim 18 (new): The method of claim 10, wherein the respective predistorting coefficients used in the combining step come from a microcontroller performing a search algorithm.